REMARKS

Claims 5-11 and 50-62 are all the claims presently being examined in the application. New claims 50-62 have been added to more particularly define the invention. Claims 12-49 have been canceled above without prejudice or disclaimer.

Claims 5-11 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-6 of U.S. Patent No. 6,252,271.

Claims 5 and 8-11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamazaki, et al. (U.S. Patent No. 5,633,519). Claims 5 and 8-11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yang (U.S. Patent No. 5,258,634). Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki, et al. in view of Wake (U.S. Patent No. 5,338,953). Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang in view of Wake. Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki, et al. Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang.

These rejections are respectfully traversed in view of the following discussion.

It is noted that the amendments are made only to more completely define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by claim 1, is directed to a a memory.

The memory includes a gate conductor including a first side and a second side where the first side includes a slope and the second side includes a substantially vertical sidewall, and

at lease one floating gate includes polysilicon spacer material and formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. (See Page 3, lines 15–25; Page 8, line 27-Page 9, line 12; and Page 11, lines 1-5 and 22-27; and Figures 1-7, 8A, 8B, 10A and 10B).

Conventional memory cell structures include a floating gate defined by a trim mask or polysilicon spacers formed on both sidewalls using an "added-on floating gate." However, the conventional structures tend to increase lithographic alignment problems, "require good control of the overlay for the spacer removal mask," prevent down-scaling of "large cell sizes," add extra process steps and materials, and thus increases manufacturing costs. (See Page 1, line 17-Page 2, line 30).

An aspect of the invention includes a floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides, which supports self-alignment and "minimizes alignment concern for high density device integration" as well as provides for the floating gate to

be "fabricated to an extremely small size and is self-isolated from adjacent FG [floating gate] devices by the gate conductor." (See Page 3, line 1-Page 4, line 2).

As a result of this invention, the resultant structure is formed using less steps and material, and thus reduces manufacturing costs. (See Page 3, lines 13-16; Page 4, lines 1-8).

II. THE OBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION

A. The Obvious-Type Double Patenting Rejection Based on U.S. Patent No. 6,252,271

First, the Examiner is prohibited from reading limitations from the specification into the applied patent claims. Accordingly claims 1-6 of Patent No. 6,252,271 B1 do not make Applicant's invention obvious. Claims 1-5 of '271 indicate, in part, that "a second sidewall having, a second slope angle greater than said first slope angle" and "at least one floating gate is partially surrounded on a plurality of sides by said second sidewall."

In contrast, the plain language of claim 5 of Applicant's invention indicates, in part, that "the first side includes a slope and the second side includes a substantially vertical sidewall and at least one floating gate which includes comprising polysilicon spacer material and formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides." Nowhere does the '271 Patent indicate "a substantially vertical sidewall" or "the gate conductor surrounds at least one floating gate." Therefore, as indicated above, the claims of the'271 Patent does not make Applicant's invention obvious.

In addition, Applicant further traverses the obviousness-type double patenting rejection based on claims 1-6 of U.S. Patent No. 6,252,271. In particular, Applicant's present invention is

a Divisional Application of U.S. Patent Application 09/097,515 (Parent Application), filed on June 15, 1998, which issued as Patent No. 6,252,271. Applicant elected to file the Divisional Application for claims 5-11 as the Examiner previously indicated that claims 5-11 of the Parent Application represented a different invention than the invention defined by claims 1-4 of the same Parent Application, which issued as U.S. Patent No. 6,252,271, with claims 1-6. Since claims 1-4 and 5-11 of the Parent Application were considered to be two different inventions, the two sets of claims cannot now represent the same invention, and thus Applicant traverses the obvious-type double patenting rejection.

III. PRIOR ART REJECTIONS

A. The Yamazaki, et al. Reference

Regarding claims 5 and 8-11, Yamazaki, et al. ("Yamazaki") fails to teach or suggest the features of independent claim 5, including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. (See Page 3, lines 15–25; Page 8, line 27-Page 9, line 12; and Page 11, lines 1-5 and 22-27; and Figures 1-7, 8A, 8B, 10A and 10B).

Instead, Figures 1(A)-1(B) and 3(E) as well as Figures 7(A), 7(B), 8(A) and 8(B) of Yamazaki teach a non volatile floating gate semiconductor including a floating gate and a control gate formed on a sidewall. In particular, this structure actually forms a double sidewall where the floating gate is formed without use of a sloped sidewall, and thus the floating gate is not self-aligned. Based on this vertical structure, the source and drain regions are formed on different

levels. (See Yamazaki at Abstract; Column 5, lines 15-22; Column 12, lines 24-40; and Figures 1(A)-1(B), 3(E), 7(A), 7(B), 8(A) and 8(B)). Accordingly, this non-volatile floating gate is a symmetric structure with a floating gate and a control gate formed "with the gate extending beyond the lower edge of the floating gate electrode," compared to just a floating gate formed on a side of a gate conductor where the other side of the gate conductor includes a sloped surface as recited in Applicant's invention. However, Yamazaki does not disclose or teach including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides as recited in Applicant's invention.

In contrast, Applicant's memory structure includes a gate conductor with a first side and a second side. The first side is sloped and the second side is a substantially vertical sidewall.

For example, in the exemplary embodiment, a floating gate of a polysilicon spacer material is formed on the second side of the gate conductor where the gate conductor surrounds the floating gate. In particular, "a notch is formed in a sidewall of the control gate, as shown in Figure 8C," such that the floating gate is surrounded by the control gate. (See Page 9, lines 8-12 and line 27 - Page 10, line 15; and Figures 8A-8D). As indicated, the floating gate is formed on the gate conductor (e.g., control gate) to yield a single sidewall structure, for example, as recited in new claim 50. Consequently, "(1) the tunneling oxide is located away from the gate (e.g., the control gate) and close to the drain area; and (2) the nitride between the control gate and floating gate is protected by the first spacer during the nitride removal step." Accordingly, the source and drain are formed on the same level, for example, as recited in new claim 51. Based on this

configuration, including the sloped or "tapered" sidewall of the first side, "the floating gates can be isolated with no additional masks," for example, as recited in new claim 52, so that the floating gate is formed on the gate conductor without a control gate. (See Page 6, lines 8-12).

Accordingly, the floating gate, itself, is formed on the gate conductor where the gate conductor (e.g., control gate) surrounds the floating gate as a result of the notching process whereas Yamazaki teaches a floating gate and a control gate formed on the sidewall to produce a double sidewall. However, Yamazaki does not disclose or teach including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. Therefore, Applicant's invention is specifically configured to support self-alignment and "minimize alignment concern for high density device integration" as well as provide for the floating gate to be "fabricated to an extremely small size and is self-isolated from adjacent FG [floating gate] devices by the gate conductor." (See Page 3, line 1-Page 4, line 2).

Accordingly, the Yamazaki structure teaches a non volatile floating gate semiconductor including a floating gate and a control gate formed on a sidewall. Thus, Yamazaki's structure is not specifically configured to support self-alignment and "minimize alignment concern for high density device integration." (See Page 3, line 1-Page 4, line 2).

Indeed, Yamazaki is focused on "forming a protruded part on a semiconductor substrate, to define the side surface of the protruded part as a region to form a channel, and to define the top part thereof one of impurity region (source or drain), while the other impurity region is provided on the bottom, so as to form a gate electrode on the side surface of the region to form a channel."

Thus, Yamazaki attempts to reduce the number of mask processes and the required accuracy of the mask processes. (Column 4, lines 5-35).

Nonetheless, the Yamazaki structure is similar to other conventional structures and may tend to increase lithographic alignment problems, "require[s] good control of the overlay for the spacer removal mask," prevent down-scaling of "large cell sizes," adds extra process steps and materials, and thus increase manufacturing costs. (See Page 1, line 17-Page 2, line 30).

Accordingly, Yamazaki only discloses a MOS type semiconductor with a floating gate and a control gate formed on a side surface. Thus, the Applicant traverses the assertion that Yamazaki teaches Applicant's invention of claim 5, and related dependent claims 8-11.

B. The Yang Reference

Regarding claims 5 and 8-11, Yang ("Yang") also fails to teach or suggest the features of independent claim 5, including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. (See Page 3, lines 15–25; Page 8, line 27-Page 9, line 12; and Page 11, lines 1-5 and 22-27; and Figures 1-7, 8A, 8B, 10A and 10B).

Instead, Figures 5C-8 of Yang teach an electrically erasable read only memory cell array having an elongated control gate in a trench. In particular, at least one floating gate is formed in the trench with a second insulating layer formed over the floating gate electrode and "a second polycrystalline layer is deposited in overlying relation to gates in trench, ..., [T]wo different configurations of layer, which will serve as a control gate." Accordingly, "[t]his leaves a gate

electrode that extends substantially the length of the trench in overlying relation to floating gates. This structure actually forms a double sidewall where the floating gate is formed without use of a sloped sidewall, and the floating gate may not be self-aligned. Further, based on this structure, the source and drain regions are formed on different levels. (See Yang at Abstract; Column 2, line 60 - Column 3, line 45; and Figures 5(A)- 8). Accordingly, this memory cell array is a symmetric structure with a floating gate and a control gate formed in a trench compared with just a floating gate formed on a side of a gate conductor where the other side of the gate conductor includes a sloped surface as disclosed by Applicant's invention. However, Yang does not disclose or teach including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides as recited in Applicant's invention.

In contrast, Applicant's memory structure includes a gate conductor with a first side and a second side. The first side is sloped and the second side is a substantially vertical sidewall. A floating gate of a polysilicon spacer material is formed on the second side of the gate conductor where the gate conductor surrounds the floating gate. (See above). In particular, "a notch is formed in a sidewall of the control gate, as shown in Figure 8C," such that the floating gate is surrounded by the control gate. (See Page 9, lines 8-12 and line 27 - Page 10, line 15; and Figures 8A-8D). As indicated, the floating gate is formed on the gate conductor, i.e., control gate, to yield a single sidewall structure, for example, as recited in new claim 50. Consequently, "(1) the tunneling oxide is located away from the gate (e.g., the control gate) and close to the drain area; and (2) the nitride between the control gate and floating gate is protected by the first

spacer during the nitride removal step." Accordingly, the source and drain are formed on the same level, for example, as recited in new claim 51. Based on this configuration, including the sloped or "tapered" sidewall of the first side, "the floating gates can be isolated with no additional masks," for example, as recited in new claim 52, so that the floating gate is formed on the gate conductor without a control gate. (See Page 6, lines 8-12).

Accordingly, the floating gate, itself, is formed on the gate conductor where the gate conductor, i.e., control gate, surrounds the floating gate as a result of the notching process whereas Yang teaches a floating gate and a control gate formed in a trench to produce a double sidewall structure. However, Yang does not disclose or teach including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. Therefore, Applicant's invention is specifically configured to support self-alignment and "minimize alignment concern for high density device integration" as well as provide for the floating gate to be "fabricated to an extremely small size and is self-isolated from adjacent FG [floating gate] devices by the gate conductor." (See Page 3, line 1-Page 4, line 2).

Accordingly, the Yang structure teaches an electrically erasable read only memory cell array including an elongated control gate where, in particular, a floating gate and a control gate are formed in a trench to form a double sidewall type structure. Thus, Yang structure is not specifically configured to support self-alignment and "minimize alignment concern for high density device integration." (See Page 3, line 1-Page 4, line 2).

Indeed, Yang is focused on an EPROM cell capable of providing a means to increase the

density and number of cell array devices and memory cells on a semiconductor chip. (Yang at Abstract; and Column 1, lines 10-45).

Nonetheless, the Yang structure is similar to other conventional structures and may tend to increase lithographic alignment problems, "require[s] good control of the overlay for the spacer removal mask," prevent down-scaling of "large cell sizes," adds extra process steps and materials, and thus increase manufacturing costs. (See Page 1, line 17-Page 2, line 30).

Accordingly, Yang only discloses an electrically erasable read only memory cell array including an elongated control gate where, in particular, a floating gate and a control gate are formed in a trench. Thus, the Applicant traverses the assertion that Yang teaches Applicant's invention of claim 5, and related dependent claims 8-11.

C. The § 103(a) Rejection of Claim 6

To make up for the deficiencies of Yamazaki and Yang, the Examiner relies on Wake ("Wake"). Wake fails to do so.

First, Wake, which pertains to "an electrically erasable and programmable semiconductor memory device having an improved writing efficiency, does not have the same aim as Yamazaki, as discussed above, and the urged combination would not have been made, absent hindsight. (See Wake at Abstract; Column 1, lines 10-20; and Column 4, lines 24-30). Applicant asserts that Yamazaki, as indicated above, in part, is a non-volatile floating gate semiconductor device focused on reducing the number of mask processes and the required accuracy of the mask processes whereas Wake's electrically erasable and programmable semiconductor memory

device includes an improved writing efficiency. Thus, the two references teach against being combined.

Similarly, Wake, as indicated above, does not have the same aim as Yang, as discussed above, and the urged combination would not have been made, absent hindsight. (See Yang at Abstract; Column 1, lines 10-245). Applicant asserts that Yang, as indicated above, in part, is an EPROM cell capable of providing a means to increase the density and number of cell array devices and memory cells on a semiconductor chip. (Yang at Abstract; and Column 1, lines 10-45) whereas Wake's electrically erasable and programmable semiconductor memory device includes an improved writing efficiency. Thus, the two references teach against being combined.

Secondly, Wake does not disclose, teach or suggest, including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides, as recited in independent claim 5.

Further, Wake does not disclose, teach or suggest, including the gate conductor which is formed on a silicon substrate, and adjacent ones of at least one floating gate are isolated from each other and the second sidewall includes tapered regions provided between the adjacent one of at least one floating gate as recited in claim 6 of the invention.

Instead, Figures 3 and 18 of Wake teaches an electrically erasable and programmable semiconductor memory device with a trench memory transistor where a floating gate electrode is formed on a first gate oxide film and a second gate oxide film in a trench. Further, "[a] control gate electrode is formed over [the] floating gate electrode with layer insulating film therebetween." In particular, "[a] pair of memory transistors M is formed in each trench.

Memory transistor M includes floating gate electrode, control gate electrode, n+ -drain diffusion region and n+ -source diffusion region." (See Wake at Abstract; Column 7, lines 20-35; and Column 8, lines 37-47). Accordingly, Wake teaches a floating gate and a control gate formed in a trench to produce a double sidewall structure whereas Applicant teaches that the floating gate, itself, is formed on the gate conductor where the gate conductor, i.e., control gate, surrounds the floating gate as a result of the notching process.

Indeed, this electrically erasable and programmable semiconductor memory device is primarily focused on providing an improved writing efficiency. (See Column 4, lines 24-40). Since this programmable semiconductor memory device includes a floating gate and a control gate in a trench to form a double sidewall type structure but does not include a floating gate includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides, Wake is deficient and thus does not teach the specific limitations of dependent claim 6.

For the reasons stated above, the claimed invention, and the invention as cited in independent claim 5, and related dependent claim 6, should be fully patentable over the cited references.

D. The § 103(a) Rejection of Claim 7 over Yamazaki, et al.

Regarding claim 7, Yamzaki, as discussed above, does not disclose, teach or suggest, including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides, as recited in independent claim 5.

Further, Yamazaki does not disclose, teach or suggest, including the gate conductor

surrounds at least one floating gate on only two sides as recited in claim 7 of the invention.

Since the Examiner admits that Yamazaki "does not disclose the gate conductor surrounds [the] at least one floating gate on only two sides,"certainly, this non-volatile floating gate semiconductor device, which includes a floating gate and a control gate formed on a side surface to produce a double sidewall type structure, does not include at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. (See Office Action, Page 7, Section 8). Accordingly, Yamazaki is deficient and thus does not teach the specific limitations of dependent claim 7.

For the reasons stated above, the claimed invention, and the invention as cited in independent claim 5, and related dependent claim 7, should be fully patentable over the cited reference.

E. The § 103(a) Rejection of Claim 7 over Yang

Regarding claim 7, Yang, as discussed above, does not disclose, teach or suggest, including at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides, as recited in independent claim 5.

Further, Yang does not disclose, teach or suggest, including the gate conductor surrounds at least one floating gate on only two sides as recited in claim 7 of the invention.

Since the Examiner admits that Yang "does not disclose the gate conductor surrounds [the] at least one floating gate on only two sides,"certainly, this non-volatile floating gate semiconductor device, which includes a floating gate and a control gate formed on a side surface

to produce a double sidewall type structure, does not include at least one floating gate which includes polysilicon spacer material formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. (See Office Action, Page 8, lines 1-6). Accordingly, Yang is deficient and thus does not teach the specific limitations of dependent claim 7.

For the reasons stated above, the claimed invention, and the invention as cited in independent claim 5, and related dependent claim 7, should be fully patentable over the cited reference.

IV. FORMAL MATTERS AND CONCLUSION

The title has been amended to be more indicative of the invention to which the claims

In view of the foregoing, Applicant submits that claims 5-11 and 50-62, all the claims presently being examined in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

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